

## Features:

- 622.08 MHz SAW-based LVPECL output
- RoHS Compliant
- Low Profile Surface Mount Package
- Excellent solder reflow performance
- PCB Substrate for excellent TCE match

## Description and applications:

Surface mount 15.9 mm SQ frequency translator operating at a 3.3V supply with complementary LVPECL outputs for use in telecom & datacom

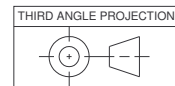
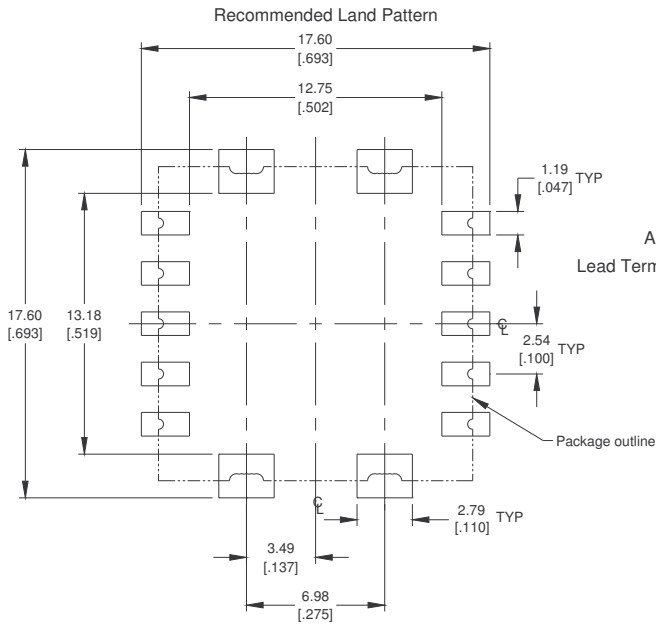
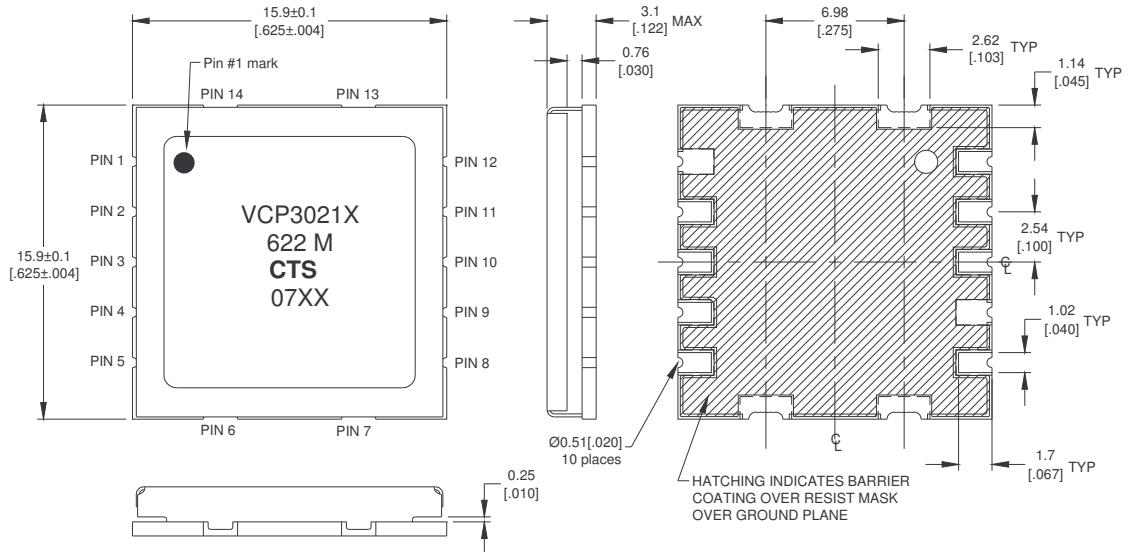


- See [WWW.CTSCORP.COM](http://WWW.CTSCORP.COM) for product patent status.

## Electrical Specifications:

VCP3021X	Specification									
Input frequency	19.440 MHz									
Output frequency	622.08 MHz									
Supply Voltage ( $\pm 5\%$ )	3.3V									
PECL input	400 mV min. peak-to-peak									
PECL output	<table border="1"> <thead> <tr> <th></th> <th>Min.</th> <th>Max.</th> </tr> </thead> <tbody> <tr> <td>Logic "0"</td> <td>1.49V</td> <td>1.68V</td> </tr> <tr> <td>Logic "1"</td> <td>2.28V</td> <td>2.42V</td> </tr> </tbody> </table>		Min.	Max.	Logic "0"	1.49V	1.68V	Logic "1"	2.28V	2.42V
	Min.	Max.								
Logic "0"	1.49V	1.68V								
Logic "1"	2.28V	2.42V								
Rise/Fall time (20% to 80%)	250 psec typical 400 psec max									
Output Duty Cycle	45/% min., 55% max.									
Current Drain	95 mA max.									
Operating Temperature	-40 to 85 °C									
Input frequency tracking capability	+/- 32 ppm minimum									
Jitter attenuation	> 3 dB @ 100 Hz offset > 30 dB @ 1 kHz offset									
Phase jitter generation, peak to peak	3 psec typical 5 psec max									
RMS phase jitter generation (1 kHz to 80 MHz)	< .5 psec typical < 1 psec max.									

**Mechanical Dimensions (mm):**  
**15.9mm x 15.9mm x 3.1mm (max.):**



All dimensions are in MM [Inches].  
 All dimensions are nominal unless otherwise specified.  
 Lead Termination Finish: Gold Flash, <10 micro inch, over Ni plated Cu.

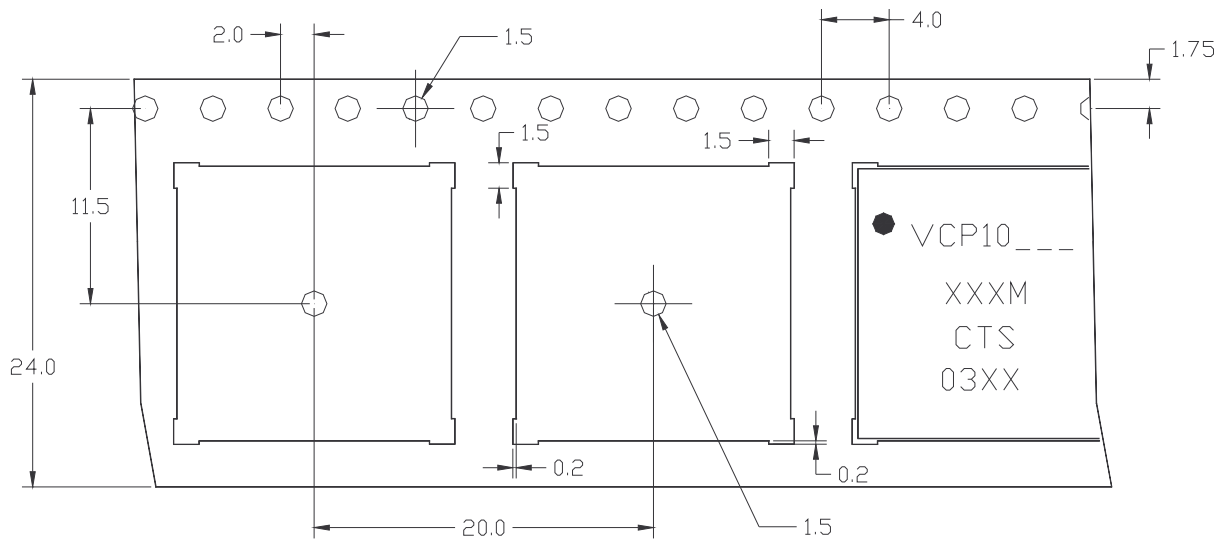
**PIN OUT**

Pin	Symbol	Function
1	LD	Lock detect Logic "1" indicates a locked condition (CMOS level $\geq V_{dd}-0.04$ ) Logic "0" indicates that no input signal is present or the input signal has moved out of the lock range (CMOS Level $\leq 0.4V$ )
2	IN	Input frequency
3	/IN	NC: not connected internally
4	GND	Ground
5	E/D	Enable/ disable Logic "0" = output disabled (CMOS Level $\leq 0.4V$ ) Logic "1" = output enabled (CMOS Level $\geq V_{dd}-0.4 V$ )
6	Gnd	Ground
7	Gnd	Ground
8	/OUT	Complementary output
9	OUT	Output
10	Vcc	Power supply voltage
11	N/C	No connection
12	Gnd	Ground
13	Gnd	Ground
14	Gnd	Ground

**Tape & Reel Information**

**Tape width 24 mm, pitch 20 mm, as per EIA 481-2, 1000 units per reel max**

All Dimensions are in MM



**Environmental Limits:**

<b>Storage Temperature</b>	<b>-40 to +90 °C.</b>
<b>Humidity</b>	<b>95% Relative humidity max @ 70°C.</b>
<b>Vibration</b>	<b>10 to 60 Hz with double amplitude of 1.52mm max. (1/2 hour in each of 3 perpendicular planes).</b>
<b>Mechanical Shock</b>	<b>1/2 sine pulse, 3000G, with pulse width 0.3mSec. (3 shock in each of 6 directions of 3 perpendicular planes).</b>

**Solder Reflow Conditions:**

Device is capable of withstanding reflow of 260 degrees C for 10 seconds maximum.

**Moisture Sensitivity: MSL 1**

**RoHS:** This device is fully compliant to RoHS Directive 2002/95/EC.